This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of claims:

1. (Currently Amended) A method for correcting the direct current offset portion (DC offset) of a first signal comprising the steps of:

phase shifting said first signal for obtaining a second signal,

comparing said first signal and said second signal with an estimated DC offset,

adjusting the estimated DC offset when ~~if~~ the first signal and the second signal are found to be on different amplitude sides of said estimated DC offset, wherein the estimated DC offset is increased when ~~if~~ the second signal is higher than the estimated DC offset and is decreased when ~~if~~ the second signal is lower than the estimated DC offset.

2. (Currently Amended) A method according to claim 1, wherein said estimated DC offset is adjusted when ~~if~~ the result of the comparison is that said first signal and said second signal are on different amplitude sides of said estimated DC offset.

3. (Currently Amended) A method according to claim 1, wherein said estimated DC offset is kept constant when ~~if~~ the result of the comparison is that said first signal and said second signal are both higher than or are both lower than estimated DC offset.

4. (Previously presented) A method according to claim 1, wherein said phase shifted second signal is obtained by low pass filtering said first signal.

5. (Previously presented) A method according to claim 1, wherein the method is used for correcting the DC offset portion of a received and demodulated radio frequency signal.

6. (Previously presented) A method according to claim 5, wherein said demodulation is a demodulation for GFSK modulated signals.

7. (Currently Amended) A device for correcting the direct current offset portion (DC offset) of a first signal comprising:

an input for connecting to a signal line for receiving said first signal,

a phase shifting element connected to the input for producing a phase shifted second signal,

means for providing an estimated DC offset, wherein said estimated DC offset is adjusted when ~~if~~ said phase shifted second signal is connected to an input of said means and said estimated DC offset is held constant when ~~if~~ said phase shifted second signal is disconnected from the input of said means,

an output signal line connected to the output of said means for providing said estimated DC offset,

a decision circuit for deciding whether ~~if~~ said first signal and said phase shifted second signal are on different or same amplitude sides of said estimated DC offset, and

a switch for connecting said phase shifted second signal to the input of said means when ~~if~~ said decision circuit decides that said first signal and said phase shifted second signal are on different amplitude sides of said estimated DC offset and disconnecting said phase shifted second signal from the input of said means when ~~if~~ the decision circuit decides that said first signal and said phase shifted second signal are on the same side of said estimated DC offset.

8. (Previously presented) A device according to claim 7, wherein said means for phase shifting said first signal is a low pass filter.

9. (Previously presented) A device according to claim 7, wherein said means for providing said estimated DC-offset is a low pass filter.

10. (Previously presented) A device according to claim 7, wherein said decision circuit comprises:

a first comparator circuit and a second comparator circuit each having an input signal line X and an input signal line Y and comparing input signals at the signal lines X and Y, the input signal line X of the first comparator circuit is connected to an output of said phase shifting element and the input signal line X of the second comparator circuit is connected to receive the first signal and the input signal lines Y of the first and second comparator circuits are, respectively, connected to the output signal line; and an Exclusive-OR (XOR) gate comprising two input signal lines, an output of said XOR gate controlling said switch and the outputs of the first and second comparator circuits are connected to the input lines of said XOR gate.

11. (Previously Presented) A radio frequency receiver comprising a device for correcting the DC offset according to claim 7 implemented as an analog circuit as part of said receiver.

12. (Previously Presented) An electronic device comprising a device for correcting the DC offset according to claim 7 implemented as a digital hardwired logic.

13. (Previously Presented) A device according to claim 7 for correcting the DC offset of a received and demodulated radio frequency signal.

14. (Previously Presented) A transceiver comprising a device for correcting the DC offset according to claim 7.

15. (Previously Presented) A communication device comprising a device for correcting the DC offset according to claim 7.